DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-8, 10-11, 13-20 and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, 20 and 26 recite the limitation "an unreacted portion of the SiGe surface layer" in lines 6-7, line 12, and line 6 respectively. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 15-16, 18 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,632,729 to Paton in view of U.S. Pat. No. 6,909,151 to Hareland et al. (Hareland).

Regarding claim 1, Paton discloses a method of forming a semiconductor device, the method comprising:

providing a substrate (Fig 1 Si-containing substrate);

forming a SiGe surface layer (within Si-containing substrate, col 3 lines 53-54) on the substrate;

depositing a high-k dielectric layer (Fig 1 "high-k gate oxide layer", col 2 lines 9-13) onto the SiGe surface layer; and

forming an oxide layer (Fig 1 "low-K SiO2 layer", col 2 lines 40-44) between the high-k dielectric layer and an unreacted portion of the SiGe surface layer by oxidizing a surface portion of the SiGe surface layer (col 2 lines 36-39), the oxide layer being formed during one or both of said depositing and an annealing process after said depositing (during anneal, col 2 lines 30-44)

forming an electrode layer (Fig 1 "gate") on the high-k dielectric layer.

Paton fails to explicitly disclose forming the SiGe surface layer having an average Ge content less than about 10 at.%. Hareland discloses SiGe surface layer having an average Ge content less than about 10 at.% (less than 25%, col 9 lines 22-24). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Paton to have SiGe surface layer having an average Ge content less than about 10 at.%. as in Hareland in order to modify device properties such as enhancement of carrier mobility to improve device performance.

Regarding claim 2, Paton in view of Hareland discloses the method according to claim 1 as above. Paton fails to disclose the substrate provided with an initial oxide layer. Hareland also discloses the substrate provided with an initial oxide layer (Figures 5A-5E, element 506, col 9 lines 9-12) prior to forming the SiGe (508/520) surface layer. It would have been obvious to one of ordinary

skill in the art at the time the invention was made to modify Paton to have an initial oxide as in Hareland in order to provide for improved device isolation.

Regarding claim 3, Paton in view of Hareland discloses the method according to claim 1 as above. Paton also includes forming the SiGe surface layer by performing thermal chemical vapor deposition, plasma-enhanced chemical vapor deposition, atomic layer deposition, or sputtering (chemical vapor deposition, col 2 lines 10-13).

Regarding claim 15, Paton in view of Hareland discloses the method according to claim 1 as above. Paton also discloses the high-k dielectric layer comprises at least one of HfO_2, $HfSiO_x$, ZrO_2, $ZrSiO_x$, TiO_2, Ta_2O_5, Al_2O_3, or SiN (col 1 lines 65- col 2 lne 9).

Regarding claim 16, Paton in view of Hareland discloses the method according to claim 1 as above. Paton also discloses the high-k dielectric layer is between about 5 – 60 angstroms thick (40-100 Å, which includes range of 40-60 Å col 2 line 59).

Regarding claim 18, Paton in view of Hareland discloses the method according to claim 1 as above. Paton fails to disclose etching the elecltoryde and high-k dielectric layer. Hareland also discloses etching the electrode layer and the high-k dielectric layer (col 11, lines 42-46). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Paton to etch the electrode layer and high-k dielectric layer in order to form devices on the substrate.

Regarding claim 26, Paton discloses a method of forming a semiconductor device, the method comprising:

providing a single crystal silicon or polycrystalline silicon substrate (Fig 1 Si-containing substrate, col 3 lines 51-52);

forming a SiGe surface layer (within Si-containing substrate, col 3 lines 53-54) on the substrate;

depositing a high-k dielectric layer (Fig 1 "high-k gate oxide layer", col 2 lines 9-13) onto the SiGe surface layer;

forming an oxide layer (Fig 1 "low-K SiO2 layer", col 2 lines 40-44) between the high-k dielectric layer and an unreacted portion of the SiGe surface layer (col 2 lines 36-39), the oxide layer being formed during one or both of said depositing and an annealing process after said depositing (during anneal, col 2 lines 30-44); and

forming an electrode layer (Fig 1 "gate") on the high-K dielectric layer.

Paton fails to explicitly disclose the SiGe surface layer having an average Ge content less than about 10 at.%. Hareland discloses a SiGe surface layer having an average Ge content less than about 10 at.% (less than 25%, col 9 lines 22-24). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Paton to have SiGe surface layer having an average Ge content less than about 10 at.%. as in Hareland in order to modify device properties such as enhancement of carrier mobility to improve device performance.

Claims 4-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,632,729 to Paton in view of U.S. Pat. No. 6,909,151 to Hareland et al. (Hareland) and in view of EP 0684 650 B1 to Hiroshi et al. (Hiroshi) as cited in IDS filed 03/10/2004.

Regarding claims 4-5, Paton in view of Hareland discloses the method according to claim 1 as above. Paton in view of Hareland fails to disclose forming the SiGe surface layer by exposing the substrate to a process gas including a Ge-containing gas comprising at least one of GeH_4 or $GeCl_4$. Hiroshi includes forming the SiGe surface layer by exposing the substrate to a process gas including a Ge-containing gas comprising at least one of GeH_4 or $GeCl_4$ (GeH_4, paragraph [0046]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Paton to have the form the SiGe surface layer as in Hiroshi to provide a high quality SiGe layer.

Regarding claim 6, Paton as modified discloses the method according to claim 4 as above. Paton discloses annealing the substrate either during said exposing, after said exposing, or both during and after said exposing (col 2 lines 30-44).

Regarding claims 7-8, Paton in view of Hareland discloses the method according to claim 4 as above. Paton in view of Hareland fails to disclose the process gas comprising a Si-containing gas comprising at least one of SiH_4, Si_2H_6, or SiH_2Cl_2. Hiroshi includes the Si-containing gas comprising at least one of SiH_4, Si_2H_6, or SiH_2Cl_2 (Si_2H_6, paragraph [0046]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to further

modify Paton to have the form the SiGe surface layer as in Hiroshi to provide a high quality SiGe layer.

Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,632,729 to Paton in view of U.S. Pat. No. 6,909,151 to Hareland et al. (Hareland) and U.S. Pub. No. 2003/0218189 to Christiansen et al. (Christiansen).

Regarding claims 10 and 11, Paton in view of Hareland discloses the method according to claim 1 above. Paton fails to disclose the SiGe surface layer comprising a plurality of SiGe sublayers each with different Ge content and also fails to disclose the SiGe surface layer comprising a graded Ge content.

Christiansen discloses a plurality of SiGe sublayers (Figure 8 layers 45, 42, 25, and 35) each with different Ge content (paragraph 82, last 3 lines) and the SiGe surface layer with a graded Ge content (Figure 9 layers 46, 37, 37 and 43, paragraph 38). It would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Paton to have the SiGe surface layer comprising a plurality of SiGe sublayers each with different Ge content and the SiGe surface layer comprising a graded Ge content as in Christiansen in order to reduce defects normally present in a single SiGe layer (Christiansen, paragraph 15).

Claims 13-14 and 19-20 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,632,729 to Paton in view of U.S. Pat. No.

6,909,151 to Hareland et al. (Hareland) and Effects of low-temperature water vapor annealing of strained SiG surface-channel pMOSFETs with high-K dielectric to Westlinder et al. (Westlinder) as cited in IDS filed 08/11/2005.

Regarding claim 13, Paton in view of Hareland discloses the method according to claim 1 as above. Paton in view of Hareland fail to explicitly disclose the SiGe surface layer is less than about 1000 angstroms thick. Westlinder also discloses the SiGe surface layer is less than about 1000 angstroms thick (10 nm, see Figure 1, which is 100 angstroms thick). It would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Paton to have the SiGe surface layer less than about 1000 angstroms as in Westlinder in order to modify device properties such as enhancement of carrier mobility to improve device performance.

Regarding claim 14, Paton in view of Hareland discloses the method according to claim 1 as above. Paton in view of Hareland fail to explicitly disclose he SiGe surface layer is between about 10 - 300 angstroms thick. Westlinder also discloses the SiGe surface layer is between about 10 - 300 angstroms thick (10 nm, see Figure 1, which is 100 angstroms thick). It would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Paton to have the SiGe surface layer between about 10 - 300 angstroms thick as in Westlinder in order to modify device properties such as enhancement of carrier mobility to improve device performance.

Regarding claim 19, Paton in view of Hareland discloses the method according to claim 1 as above including the oxide formed during an annealing

process. Paton fails to explicitly disclose the oxide layer formed by exposing the substrate to an oxygen containing gas. Westlinder discloses an oxide layer formed by exposing the substrate to an oxygen containing gas (exposed to water vapor anneal, page 526 col 1 paragraph 3, and oxygen is present in H_2O). It would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Paton to expose to oxygen gas as in Westlinder in order to control the formation of the oxide to a desired level.

Regarding claim 20, Paton discloses a method of forming a semiconductor device, the method comprising:

providing a substrate (Fig 1 Si-containing substrate);

forming a SiGe surface layer (within Si-containing substrate, col 3 lines 53-54) on the substrate;

depositing a high-k dielectric layer (Fig 1 “high-k gate oxide layer”, col 2 lines 9-13) onto the SiGe surface layer;

annealing the substrate having the SiGe and high-k dielectric thereon (anneal, col 2 lines 30-44); and

forming an electrode layer (Fig 1 “gate”) on the high-K dielectric layer.

wherein at least one of the depositing and annealing comprising to form an oxide layer (Fig 1 “low-K SiO2 layer”, col 2 lines 40-44) between the dielectric layer and an unreacted portion of the SiGe surface layer .

Paton fails to explicitly disclose the oxide layer formed by exposing the substrate to an oxygen containing gas. Westlinder discloses an oxide layer formed by exposing the substrate to an oxygen containing gas (exposed to water

vapor anneal, page 526 col 1 paragraph 3, and oxygen is present in H_2O). It would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Paton to expose to oxygen gas as in Westlinder in order to control the formation of the oxide to a desired level.

Paton fails to explicitly disclose the SiGe surface layer having an average Ge content less than about 10 at.%. Hareland discloses SiGe surface layer having an average Ge content less than about 10 at.% (less than 25%, col 9 lines 22-24) It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Paton to have SiGe surface layer having an average Ge content less than about 10 at.%. as in Hareland in order to modify device properties such as enhancement of carrier mobility to improve device performance.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,632,729 to Paton in view of U.S. Pat. No. 6,909,151 to Hareland et al. (Hareland) and U.S. Pat. No. 5,259,881 to Edwards et al. (Edwards).

Regarding claim 17, Paton in view of Hareland discloses the method according to claim 1 as above with an Si substrate. Paton in view of Hareland fails to disclose introducing the substrate into a process chamber of one of a single wafer processing system and a process chamber of a batch-type processing system. Edwards teaches introducing a substrate into a process chamber of a batch-type processing system (col 3 lines 6-13). It would have been

obvious to one of ordinary skill in the art at the time the invention was made to further modify Paton to include introducing the Si substrate into a process chamber of a batch-type processing system in order to maximize the add to the speed and flexibility of the substrate processing (Edwards, lines 14-17).

Response to Arguments

Applicant's arguments with respect to claims 1-8, 10-11, 13-20 and 26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colleen A. Matthews whose telephone number is (571)272-1667. The examiner can normally be reached on Monday - Friday 8AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C. A. M./
Examiner, Art Unit 2811

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811